DDF annual report

Title of Investigation:

Development of Copper-filled Silicon Micro-Trenches for Cooling Close-Packed X-ray Microcalorimeter Arrays

Principal Investigator:

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Initiation Year:

FY 2005

Aggregate Amount of Funding Authorized in FY 2004 and Earlier Years:

$0

Funding Authorized for FY 2005:

$52,000

Actual or Expected Expenditure of FY 2005 Funding:

In-house: $52,000

Status of Investigation at End of FY 2005:

Terminated at end of FY 2005; insufficient progress had been made to assess the appropriateness of renewing. Progress reported here was largely achieved in first quarter FY 2006.

Expected Completion Date:

December 31, 2005; later resumption possible under Constellation-X project

Purpose of Investigation:

An X-ray microcalorimeter is a device that measures the energy of individual X-rays by measuring the temperature increase resulting from their absorption. Constellation-X is a proposed X-ray astronomy satellite, which includes a 32x32 array of microcalorimeter pixels in the focal plane for imaging X-ray spectroscopy. Future X-ray imaging spectrometers, such as those needed for Constellation-X, will consist of compact megapixel arrays. With the development of large, close-packed microcalorimeter arrays, effective array cooling becomes an important issue for maintaining peak instrument performance. The purpose of this investigation was to investigate ways to increase the overall thermal conductivity and heat capacity of microcalorimeter arrays.

For Constellation-X's current array development, the silicon substrate between the pixels offers the only path by which the Joule heat from electrically biasing each pixel is carried out through the array to the heat bath. Therefore, the thermal conductance of the silicon structure has to be significantly higher than the thermal conductance of each pixel to that silicon frame to guarantee identical operational conditions throughout the array. Since the bias power of every microcalorimeter in the array flows to the same substrate, the requirement for the heat sinking of the silicon structure increases with the number of pixels. In addition to bias power dissipation, close-packed arrays can exhibit cross-talk between the pixels. The amplitude and time characteristics of these cross-talk pulses depend on the fraction of X-ray energy lost to the silicon substrate, the thermal conductivity, and the heat capacity of the substrate. To reduce cross-talk and operating point problems in large compact arrays, the thermal conductivity and the heat capacity of the substrate has to be high and scale with the size of the array. Thus, we proposed to develop copper-filled silicon microtrenches (CuMT) to dramatically increase the overall thermal conductivity and heat capacity of microcalorimeter arrays.

Accomplishments to Date:

Several test structures of copper-filled silicon microtrenches (CuMT) have been designed, fabricated, and tested. Electrical measurements and structural integrity checks have been performed between ambient temperature and 0.1 K. A first estimate on the thermal conductivity value of CuMT at very low temperatures has been obtained from experimental data.

Figure 1a shows a test chip, or cell, with two perpendicularly oriented bundles of 17 parallel CuMT. The array structure, which is created by these two bundles, has 250-micron large square pixels (see Figure 1b) simulating the pixelation of our current 8x8 microcalorimeter detector arrays. There are 36 test cells laid out on a 4-inch silicon wafer. All silicon wafers are of <100> crystal orientation. Each cell contains CuMT of only one out of three trench widths, which are 20, 40, and 60 microns. The trench depths can be tailored independently from wafer to wafer and range between 10 and 30 microns.
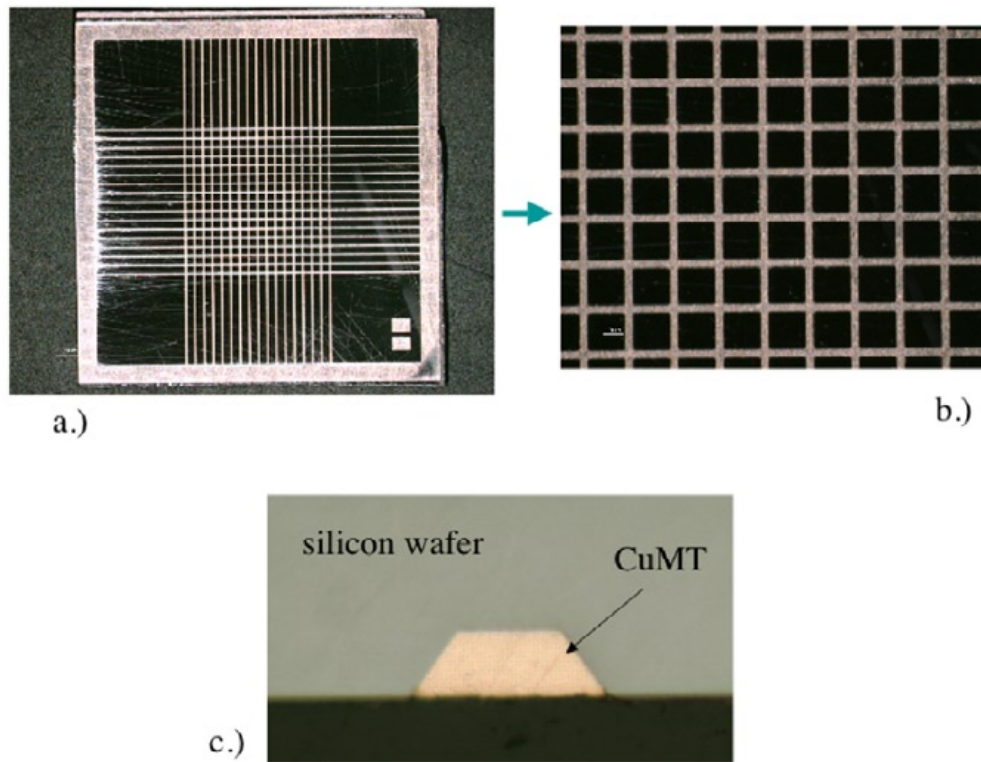
Figure 1. (a) A 1 cm x 1 cm large test chip with 40-micron wide CuMT micro-machined into a silicon surface. (b) Close-up of the center of the test chip, where the two bundles of CuMT create a 250-micron large square pixel structure simulating the pixelation used in our current 8x8 detector array design. (c) Cross-sectional micrograph of a 20-micron wide and 11-micron deep CuMT.

The fabrication of CuMT can be divided into three steps: 1) Silicon Surface Micro-Machining (SSMM), 2) Copper Electro-Deposition (CED), and 3) Wafer Planarization. As our SSMM tool, we chose a KOH-based wet silicon etch process to produce trenches with a slanted sidewall and micro-roughened surface. The best results were obtained when using a 20% KOH solution at 70°C with an etch rate of about 0.6 micron/minute. A 0.5-micron thick silicon nitride coating, which had been patterned photolithographically, was used as the etch mask. The observed maximum variation in trench depth was ±1 micron on a wafer scale. The SSMM process step was completed by growing a 0.3–0.5-micron thick thermal silicon oxide layer onto the microtrench structures to prevent potential copper atom migration from the CuMT into the adjacent silicon.

The CED process started with the thermal-vacuum deposition of a 1-micron thick copper/gold seed layer onto the wafer. Since the sidewalls of the trenches were slanted at a 54.7° angle with the wafer surface, the seed layer easily covered the whole trench profile. Complete seed layer coverage is an important prerequisite for a successful trench filling process. The actual CED took place in a dedicated copper-plating bath at Goddard's plating facility. We were using a novel Periodic Pulse-Reverse (PPR) electroplating process that we had previously developed for plating through-wafer microvias (DDF 2001). The PPR electro-deposition rate was approximately 0.2 micron/minute yielding void-free growth starting from the seed layer. Figure 1c shows a cross-sectional micrograph of a 20-micron wide and 11-micron deep CuMT.

The last step in the fabrication is the planarization of the wafer to remove excess copper from its surface. To date, we are limited to mechanical-planarization methods like lapping a wafer with fine and ultra-fine silicon oxide abrasive grids and wheels. Currently, we are developing a new procedure to improve the finish of the wafer surface.

After dicing the completed wafer, single CuMT test cells went through electrical and structural integrity tests. An Oxford Kelvinox 25 dilution refrigerator was used as a cooling platform to primarily measure the RFT (Resistance R as a Function of Temperature T) response of a CuMT and observe its structural behavior on thermal stress. Table 1 summarizes some fundamental data of a 40-micron wide and 11-micron deep CuMT, which was taken when its test chip was cooled down to 100 mK. Although a significant mismatch in thermal expansion between copper and silicon was expected, no structural failure has been observed. We were aiming for and achieved better than a factor of 6 drop in resistance at 4 K compared with 300 K.

Table 1. Electrical and thermal properties of a CuMT at different temperatures

Temperature	R(300K)/R(T)	Electr. Resistivity ρ [$\mu\Omega$ cm]	Thermal resistivity $\kappa_{est.}$ [W/K m]
300K	1	28.82	N/A
77K	2.78	7.50	N/A
4K	7.81	3.69	1.19
0.1K	7.81	3.69	0.0298

Planned Future Work:

As a next step, we intend to integrate CuMT structures in our current 8x8 microcalorimeter detector array. This will allow us to further study their thermal characteristics and quantitatively determine their impact on thermal cross-talk between detector pixels.

Key Points Summary:

Project's innovative features: Use of electroplated copper micro-heat pipes in silicon wafers is an innovative approach to the thermal design of large arrays of microcalorimeters with resistive thermometers. Joule power is dissipated in such devices when they are operated, and the micro-heat pipes were conceived to remove the bias power from a large array mounted to a 50-mK cold stage.

Potential payoff to Goddard/NASA: The thermal design of a 1024-pixel X-ray calorimeter array will be driven by the integrated bias power. Given typical bias powers of >10 pW/pixel, array heat sinks will need much higher thermal conductance than currently obtained to keep the whole die from heating and each pixel connected to the same reference temperature. The heat sinking of the XRS array for Astro-E2 was measured to be 90 nW/K. This was fine for a 32-pixel array of low-power calorimeters, but is unacceptable for Constellation-X or larger arrays.

The criteria for success: These include adequate thermal conduction along the copper, adequate thermal contact between the silicon substrate and the copper, robustness to thermal cycling, and successful integration into the fabrication process of (superconducting) Transition-Edge Sensors (TES), a type of microcalorimeter array.

Technical risk factors: The mismatch in the thermal coefficient of expansion between Cu and Si may lead these structures to fail on thermal cycling, or simply for the thermal coupling to degrade over time. There has been insufficient study time to evaluate whether this risk will ultimately prevent success.